Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-36. (Cancelled)

Claim 37. (Currently amended) ~~The integrated circuit of claim 36 further~~ An integrated circuit comprising:

a shader circuit;

a texture circuit including a texture cache coupled to the shader circuit;

a frame buffer interface coupled to the texture circuit; and

a texture descriptor cache controller coupled between the shader and the frame buffer interface,

wherein the shader requests texture descriptors from the frame buffer interface, and a plurality of texture descriptors are stored in a texture descriptor cache for use by the texture circuit, and

wherein the texture descriptor cache controller receives texture descriptor requests from the shader.

Claim 38. (Currently amended) The integrated circuit of claim ~~31~~ 37 wherein at least one of the plurality of texture descriptors is ~~retrieved~~ requested a plurality of times.

Claim 39. (Previously presented) An integrated circuit comprising:

a graphics pipeline;

a shader circuit coupled to the graphics pipeline;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the shader circuit is configured to receive a first texture descriptor, a first hint, and a first command from the graphics pipeline, the first command using the first texture descriptor,

and wherein the texture circuit is configured to receive a second texture descriptor identified by the first hint using the frame buffer interface.

Claim 40. (Previously presented) The integrated circuit of claim 39 wherein the shader is further configured to receive a first portion of a shader program including a second command and a third command, the second command using the second texture descriptor and the third command using a third texture descriptor, and

wherein the texture circuit is further configured to receive the third texture descriptor using the frame buffer interface.

Claim 41. (Previously presented) The integrated circuit of claim 40 further comprising:

a first register configured to store the first descriptor;

a second register configured to store the second descriptor; and

a third register configured to store the third descriptor.

Claim 42. (Previously presented) The integrated circuit of claim 41 wherein the shader is further configured to receive a second portion of a shader program comprising a fourth command, the fourth command using a fourth texture descriptor, and

wherein the texture circuit is further configured to receive the fourth texture descriptor using the frame buffer interface.

Claim 43. (Previously presented) The integrated circuit of claim 42 wherein the second register is further configured to store the fourth texture descriptor.

Claim 44. (Previously presented) An integrated circuit comprising:

a graphics pipeline;

a shader circuit coupled to the graphics pipeline;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the shader circuit is configured to receive a portion of a shader program including a first command, the first command using a first texture descriptor, and

wherein the first texture descriptor is prefetched before the shader executes the first command.

Claim 45. (Previously presented) The integrated circuit of claim 44 wherein the first texture descriptor is prefetched by the shader circuit.

Claims 46-54. (Cancelled)